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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/616,801	07/10/2003	Kurt Kimber	P440.12-0006	2291

164 7590 10/05/2004

KINNEY & LANGE, P.A.
THE KINNEY & LANGE BUILDING
312 SOUTH THIRD STREET
MINNEAPOLIS, MN 55415-1002

EXAMINER	
LEJA, RONALD W	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 10/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/616,801	KIMBER ET AL.	
	Examiner	Art Unit	
	Ronald W Leja	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 7-13* is/are rejected.

7)☒ Claim(s) *5,6,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/6/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 4, 7-9 and 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (6,744,611).

Yang et al. disclose a circuit for offering protection from ESD events (see Fig. 3). The circuit includes (for Claim 13), an ESD event sensor (51), which comprises a zener diode for Claim 2 and monitors a voltage magnitude for Claim 9. The circuit has a breakdown voltage adjustment circuit (40), which comprises a mirror for Claim 4; the circuit (40) receives a first signal from the ESD sensor at the gate of transistor (55) and is considered to receive a second signal

after the ESD event transpires and zener diode (51) no longer conducts (for Claims 7 and 11). See also Col. 2, lines 38-55. Yang et al. do not specifically disclose that transistor (69) is a "vulnerable device". However, it is the opinion of the Examiner that all elements on a chip, such as, transistor (69), are "vulnerable" to ESD events, and as such, it would have been obvious to offer protection to them from ESD events, thereby increasing the durability and reliability of the chip and all of its components. In this particular case, transistor (69) has its breakdown voltage adjusted so as to allow it to conduct a portion of the ESD event, thereby preventing any damage from ESD voltage level stresses occurring across its electrodes.

Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. in view of Miller et al. (5,946,177).

These claims are drawn to ESD event monitoring by rate-of-change of a voltage on a pad or use of an RC trigger. Yang et al. are silent with respect to such monitoring. Miller et al. teach the ESD event sensing via rate-of-change of the voltage wherein such is accomplished with an RC sensor (126,127). It would have been obvious to one having ordinary skill in the art at the time of the invention to incorporate the teachings of rate-of-change of voltage monitoring and incorporating use of an RC sensor, as fairly taught by Miller et al., as a means to ensure early reaction to those ESD events, which are highly transient in their front or initial wave (thus use of RC), thereby enhancing the overall ESD protection resulting in increased chip reliability and durability.

Claims 5, 6, 14 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The added limitations found in Claims 5, 6, 14 and 15 are drawn to specifics with respect to the adjusting of the breakdown voltage of the vulnerable device; such limitations in combination are not disclosed nor suggested by the Prior Art of Record.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ronald W Leja whose telephone number is (571)272-2053. The examiner can normally be reached on Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (571)272-2800. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ronald W Leja
Primary Examiner
Art Unit 2836

9/29/04

rwl
September 29, 2004